ABSTRACT OF THE DISCLOSURE

The present invention is generally directed to an apparatus and method for reducing excess power consumption of a bus master circuit component for use in a multi-bus master system. In one embodiment, the bus master is provided in the form of an integrated circuit comprising clock control logic that is configured to disable a clock signal that is otherwise delivered to functional circuitry contained within the integrated circuit during a period of time between the request for mastership of a bus and the grant of that request.